Features

- Fast Read Access Time - 150 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 256-Bytes
  - Internal Control Timer
- Fast Write Cycle Time
  - Page Write Cycle Time - 10 ms Maximum
  - 1 to 256-Byte Page Write Operation
- Low Power Dissipation
  - 80 mA Active Current
  - 300 µA CMOS Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10,000 Cycles
  - Data Retention: 10 Years
- Single 5V ± 10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-Wide Pinout
- Full Military, Commercial and Industrial Temperature Ranges

4 Megabit (512K x 8) Paged CMOS E^2PROM

Preliminary

Description

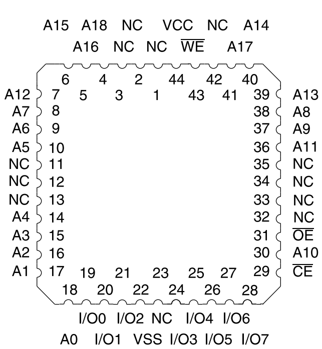
The AT28C040 is a high-performance electrically erasable and programmable read only memory (E^2PROM). Its 4 megabits of memory is organized as 524,288 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 150 ns with power dissipation of just 440 mW. When the device is deselected, the CMOS standby current is less than 300 µA.

(continued)

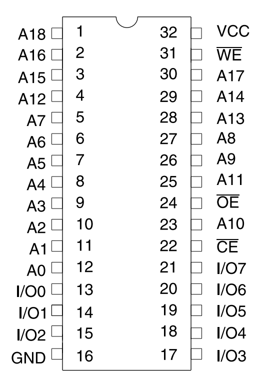
Pin Configurations

Pin Name	Function
A0 - A18	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

LCC
Top View



SIDE BRAZE, FLATPACK
Top View



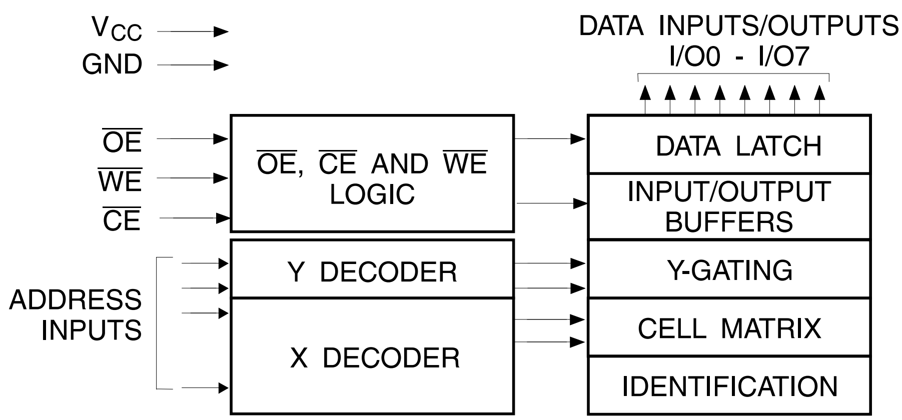
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Description (Continued)

The AT28C040 is accessed like a static RAM for the read or write cycle without the need for external components. The device contains a 256-byte page register to allow writing of up to 256-bytes simultaneously. During a write cycle, the address and 1 to 256-bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA POLLING of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

Atmel's AT28C040 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 256-bytes of E^2PROM for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C040 is accessed like a static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their systems.

BYTE WRITE: A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

PAGE WRITE: The page write operation of the AT28C040 allows 1 to 256-bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 255 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded, the AT28C040 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A8 - A18 inputs. For each $\overline{WE}$ high to low transition during the page write operation, A8 - A18 must be the same.

The A0 to A7 inputs specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

$\overline{\text{DATA}}$ POLLING: The AT28C040 features $\overline{\text{DATA}}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{\text{DATA}}$ Polling may begin at anytime during the write cycle.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ Polling, the AT28C040 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION: If precautions are not taken, inadvertent writes may occur during transitions of the host system power supply. Atmel has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION: Hardware features protect against inadvertent writes to the AT28C040 in the following ways: (a) V_{CC} sense - if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay - once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a write: (c) write inhibit - holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION: A software controlled data protection feature has been implemented on the AT28C040. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28C040 is shipped from Atmel with SDP disabled.

SDP is enabled when the host system issues a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the 3-byte command sequence and after t_{WC}, the entire AT28C040 will be protected against inadvertent write operations. It should be noted that once protected, the host can still perform a byte or page write to the AT28C040. To do so, the same 3-byte command sequence used to enable SDP must precede the data to be written.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP, and SDP will protect the AT28C040 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device, and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the 3-byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

(continued)

Device Operation (Continued)

DEVICE IDENTIFICATION: An extra 256-bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12V ± 0.5V and using address locations 7FF80H to 7FFFFH, the bytes may be written to or read from in the same manner as the regular memory array.

OPTIONAL CHIP ERASE MODE: The entire device can be erased using a 6-byte software erase code. Please see Software Chip Erase application note for details.

DC and AC Operating Range

		AT28C040-15	AT28C040-20	AT28C040-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.

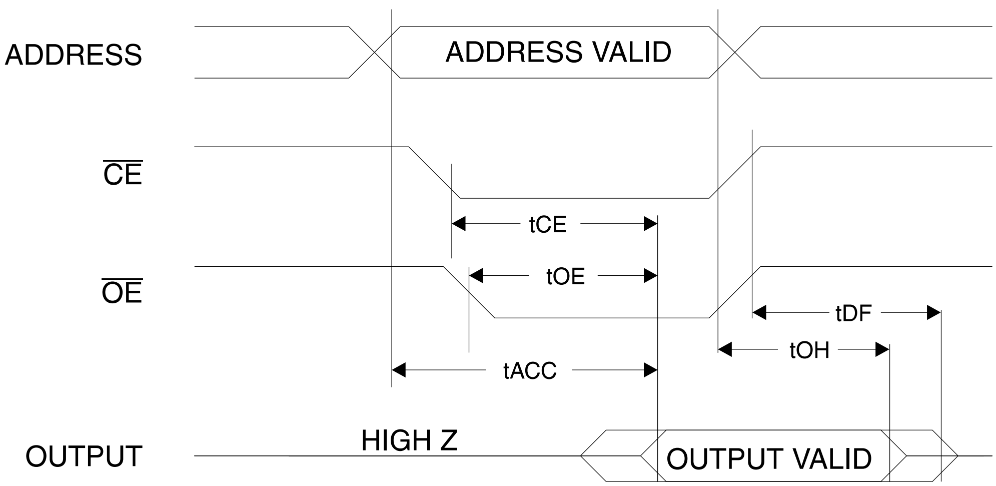
DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1V		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1V		3	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		80	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

AC Read Characteristics

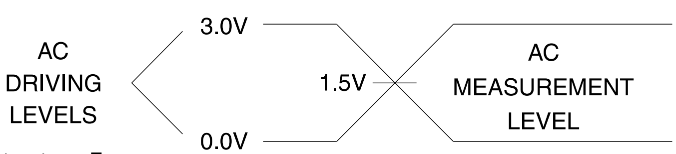
Symbol	Parameter	AT28C040-15		AT28C040-20		AT28C040-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{\text{CE}}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{\text{OE}}$ to Output Delay	0	55	0	55	0	55	ns
t_{DF} (3, 4)	$\overline{\text{CE}}$ or $\overline{\text{OE}}$ to Output Float	0	55	0	55	0	55	ns
t_{OH}	Output Hold from $\overline{\text{OE}}$, $\overline{\text{CE}}$ or Address, whichever occurred first	0		0		0		ns

AC Read Waveforms (1, 2, 3, 4)



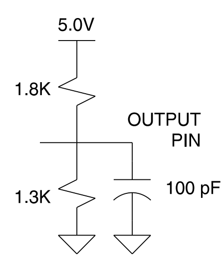
Notes: 1. $\overline{\text{CE}}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{\text{OE}}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{\text{CE}}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC} .
3. t_{DF} is specified from $\overline{\text{OE}}$ or $\overline{\text{CE}}$, whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance (f = 1 MHz, T = 25°C) (1)

	Typ	Max	Units	Conditions
C_{IN}	4	10	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

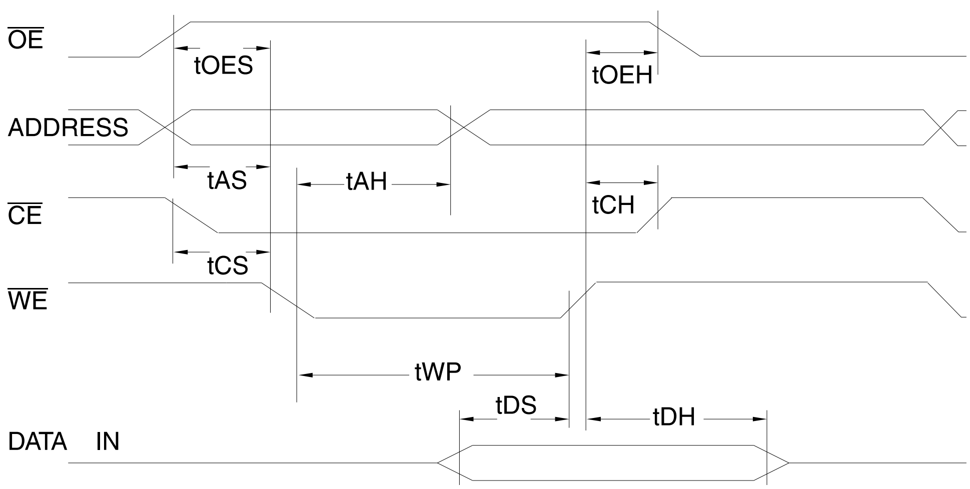
Note: 1. This parameter is characterized and is not 100% tested.

AC Write Characteristics

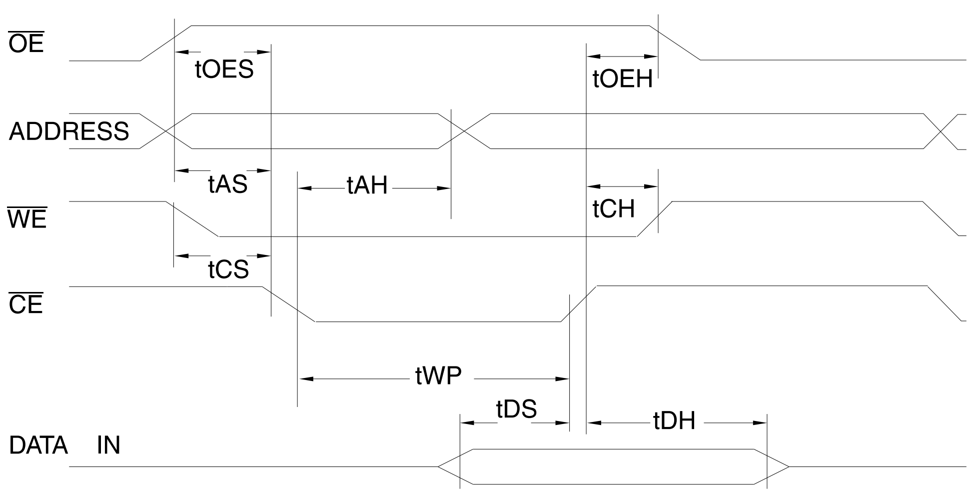
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns

AC Write Waveforms

$\overline{WE}$ Controlled



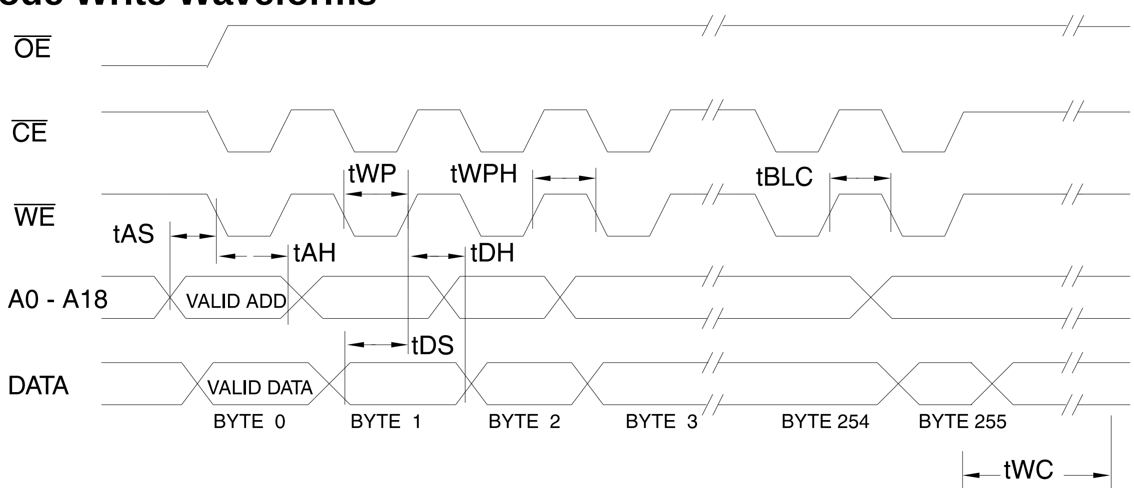
$\overline{CE}$ Controlled



Page Mode Characteristics

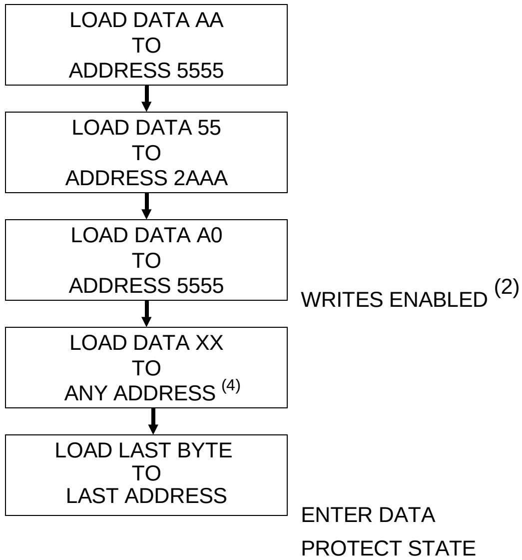
Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Set-up Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

Page Mode Write Waveforms [1, 2]



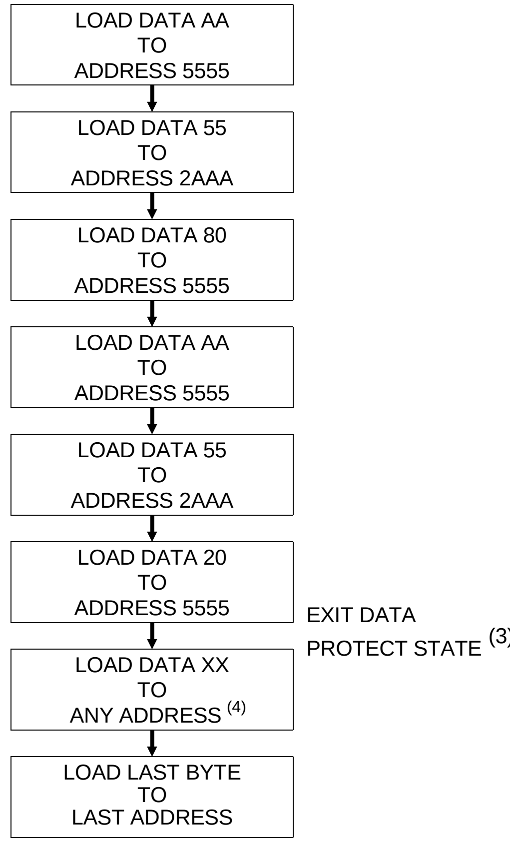
Notes: 1. A8 through A18 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when WE and CE are both low.

Software Data Protection Enable Algorithm (1)

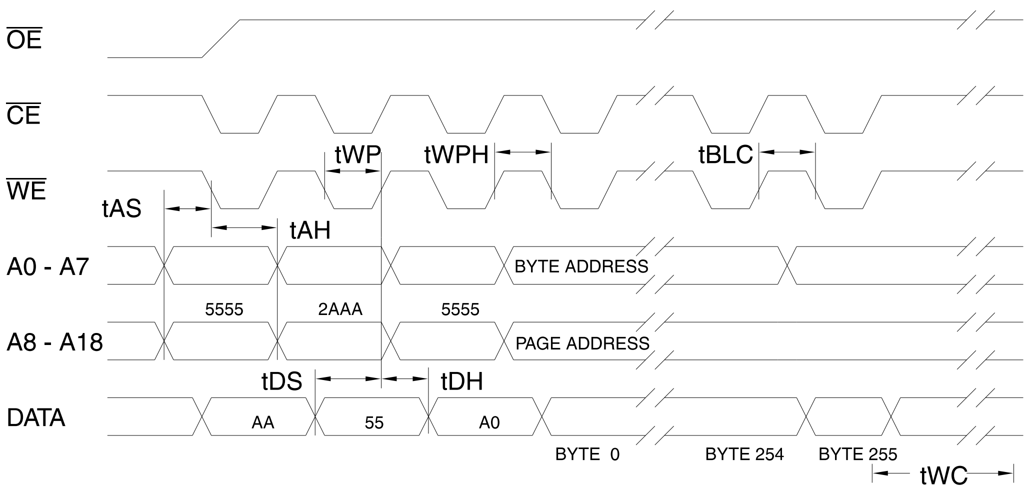


Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 256-bytes of data are loaded.

Software Data Protection Disable Algorithm (1)



Software Protected Program Cycle Waveform (1, 2, 3)



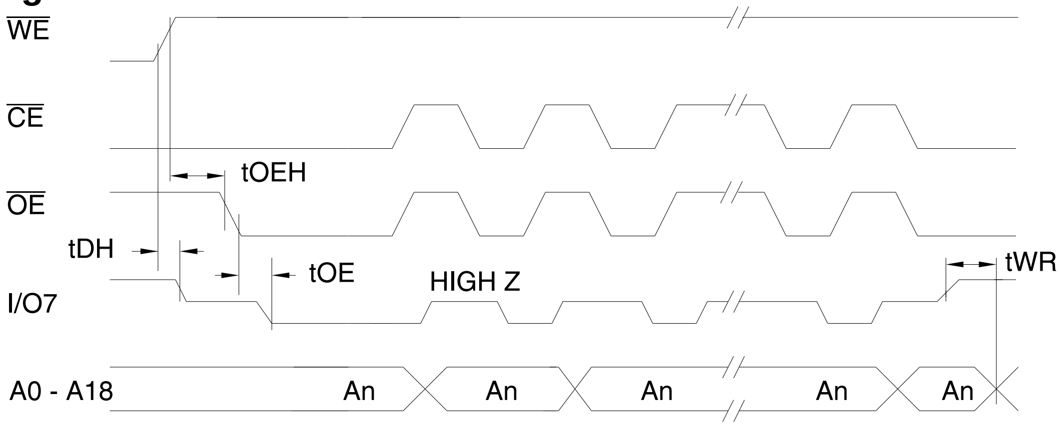
Notes:
1. A0 - A14 must conform to the addressing sequence for the first 3-bytes as shown above.
2. After the command sequence has been issued and a page write operation follows, the page address inputs (A8 - A18) must be the same for each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
3. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

$\overline{\text{Data}}$ Polling Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

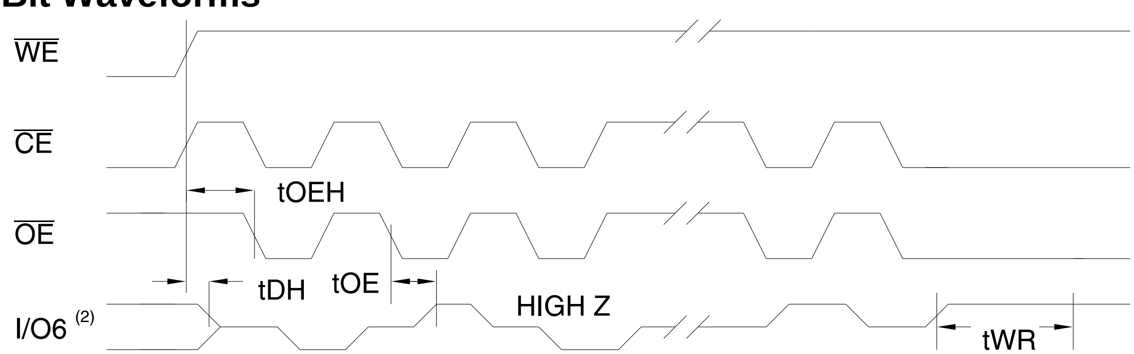


Toggle Bit Characteristics [1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay [2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

Toggle Bit Waveforms [1, 2, 3]



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Ordering Information (1)

t_{ACC} (ns)	I_{CC} (mA) Active	I_{CC} (mA) Standby	Ordering Code	Package	Operation Range
150	80	0.3	AT28C040-15BC AT28C040-15FC AT28C040-15LC	32B 32F 44L	Commercial (0° to 70°C)
	80	0.3	AT28C040-15BI AT28C040-15FI AT28C040-15LI	32B 32F 44L	Industrial (-40° to 85°C)
	80	0.3	AT28C040-15BM AT28C040-15FM AT28C040-15LM	32B 32F 44L	Military (-55°C to 125°C)
	80	0.3	AT28C040-15BM/883 AT28C040-15FM/883 AT28C040-15LM/883	32B 32F 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	80	0.3	AT28C040-20BC AT28C040-20FC AT28C040-20LC	32B 32F 44L	Commercial (0° to 70°C)
	80	0.3	AT28C040-20BI AT28C040-20FI AT28C040-20LI	32B 32F 44L	Industrial (-40° to 85°C)
	80	0.3	AT28C040-20BM AT28C040-20FM AT28C040-20LM	32B 32F 44L	Military (-55°C to 125°C)
	80	0.3	AT28C040-20BM/883 AT28C040-20FM/883 AT28C040-20LM/883	32B 32F 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	80	0.3	AT28C040-25BC AT28C040-25FC AT28C040-25LC	32B 32F 44L	Commercial (0° to 70°C)
	80	0.3	AT28C040-25BI AT28C040-25FI AT28C040-25LI	32B 32F 44L	Industrial (-40° to 85°C)
	80	0.3	AT28C040-25BM AT28C040-25FM AT28C040-25LM	32B 32F 44L	Military (-55°C to 125°C)
	80	0.3	AT28C040-25BM/883 AT28C040-25FM/883 AT28C040-25LM/883	32B 32F 44L	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Note: 1. See Valid Part Numbers on next page.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C040	15	BC, BI, FC, FI, LC, LI, BM/883, FM/883, LM/883
AT28C040	20	BC, BI, FC, FI, LC, LI, BM/883, FM/883, LM/883
AT28C040	25	BC, BI, FC, FI, LC, LI, BM/883, FM/883, LM/883

Package Type	
32B	32 Lead, 0.600" Wide, Ceramic Side Braze Dual Inline (Side Braze)
32F	32 Lead, Non-Windowed, Ceramic Bottom-Brazed Flat Package (Flatpack)
44L	44 Pad, Non-Windowed, Ceramic Leadless Chip Carrier (LCC)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms